EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Patrick Muffo (Reg. No. 60,342) on 27 February 2009.

The following claims have been amended as follows:

4. A device having a hardware interface and a logical circuit comprising a logical operation element, which defines the hardware interface, using a first interface definition language which is partly common to a second interface definition language directed to a software object, ~~wherein~~ the first interface definition language ~~has~~ having means for defining a plurality of functions, each function having a function name and a return value, and at least one function having at least one function argument, the device comprising:

~~wherein~~ a server interface circuit for realizing the interface, the server interface circuit comprising ~~comprises~~ a function identifying register for identifying the function name defined by the first interface definition language among the function identifying register for identifying the function name defined by the first interface definition language, an input/output register for storing the argument, and a return value register

for storing the return value, means for determining whether the function is the at least one function having the at least one function argument, and means for performing at least one of inputting the at least one function argument and outputting the at least one function argument, the return value being generated by a random number generator, and

~~wherein~~ the software object ~~is~~ capable of realizing the hardware interface independently of the server interface circuit by using only the second interface definition language.

11. A device having a hardware interface and a logical circuit comprising a logical operation element, which defines the hardware interface, using an interface definition language having means for defining a function name, an argument, and a return value for each function defined by the function name, ~~wherein~~ the device comprising:

a server interface circuit for realizing the interface, the server interface circuit comprising ~~comprises~~:

a function identifying register for identifying the function name defined by the interface definition language among the function identifying register for identifying the function name defined by the interface definition language, an input/output register for storing the argument, and a return value register for storing the return value, the return value being generated by a random number generator; and

an argument number detection section for determining whether the function is the at least one function having the at least one function argument, and

~~wherein~~ a client interface circuit ~~is~~ capable of realizing the interface independently of the server interface circuit by using another interface definition language~~, and~~

~~wherein the return value is generated by a random number generator~~.

12. A device having a hardware interface and a logical circuit, which defines the hardware interface, using an interface definition language having means for defining a plurality of functions, each function having a function name and a function return value, and at least one function having at least one function argument, the device comprising:

~~wherein~~ a client interface circuit for realizing the interface, the client interface circuit comprising ~~comprises~~ a function identifying register for identifying the function name defined by the interface definition language among the function identifying register for identifying the function name defined by the interface definition language, an input/output register for storing the argument, and a return value register for storing the return value, means for determining whether the function is the at least one function having the at least one function argument, and means for performing at least one of inputting the at least one function argument and outputting the at least one function argument, ~~wherein~~ the client interface circuit is capable of realizing the interface

independently of a server interface circuit by using another interface definition language, and

~~wherein~~ the ~~function~~ return value being ~~is~~ generated by a random number generator.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NATHAN PRICE whose telephone number is (571)272-4196. The examiner can normally be reached on 8:30am - 5:00pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/ NP

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